UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/698,449	11/03/2003	Masakuni Kawagoe	030712-16	3463

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EXAMINER
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ART UNIT	PAPER NUMBER
2616	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

<table>
<tr><td rowspan="2">Office Action Summary</td><td colspan="2">Application No.</td><td colspan="2">Applicant(s)</td></tr>
<tr><td colspan="2">10/698,449</td><td colspan="2">KAWAGOE ET AL.</td></tr>
<tr><td>Examiner</td><td></td><td colspan="2">Art Unit</td><td></td></tr>
<tr><td></td><td>Xavier Szewai Wong</td><td></td><td colspan="2">2616</td><td></td></tr>
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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on <u>*2nd July 2007*</u>.

2a)☒ This action is **FINAL**.   2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) <u>*1-11*</u> is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) <u>*1-11*</u> is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a)☐ All   b)☐ Some *   c)☐ None of:

      1.☐ Certified copies of the priority documents have been received.

      2.☐ Certified copies of the priority documents have been received in Application No. _____.

      3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.

4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date _____.

5) ☐ Notice of Informal Patent Application

6) ☐ Other: _____.

DETAILED ACTION

-       Applicant's Amendment filed 2nd *July 2007* is acknowledged

-       Claim **1** has been amended

-       Claims **1-11** are still pending in the present application

-       This action is made FINAL

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that

form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims **1, 2** and **4 – 8** are rejected under 35 U.S.C. 102(b) as being anticipated

by **Yoneda et al (U.S Patent 5,726,942)**.

Consider claim **1, Yoneda et al** clearly show and disclose an encoder (as an

arbiter circuit) that comprises: a timing control circuit *60* that sends variation of output

signals to show a timing at which a flag data in a prefetch circuit *16* is shifted to a flag

register *18* (col. *25* lines *39-46*; figs. *10-11*); prioritizing means are accomplished by a

priority sub-block encoder (priority circuit) that assigns signals as mismatch ("0" as in

invalid/lower priorities) or hit ("1" as in valid/highest priority) in which only a first priority

address matches even though a plurality of matching signal candidates exist as

afterwards the signals will be detected by a flag data sense circuit *126* (col. *4* lines *5-13*,

col. *11* lines *42-47* & col. *53* lines *42-46*; figs. *1-2*). When priority flag/hit data moves to

another priority sub-block, the flag data goes through a priority encode cycle (delay) in which the contents of the flag register *18* are switched over to the second priority flag data held in the prefetch circuit after the last hit signal in the flag data in the first priority sub-block held in the flag register is reset; therefore, producing a time/delay during which no encode output can be performed (col. *22* lines *7-15*). **Yoneda et al** further disclose controlling means (timing control circuit *60*) for outputting a signal to the data transfer request signal holding means (holding *m+1* of 1-bit data "0" or "1") based on the signals output from the prioritizing means (priority sub-block) (col. *21* lines *28-45* & col. *22* lines *16-34*).

Consider claim **2**, and as applied to claim **1** above, **Yoneda et al** clearly show and disclose a priority flag data goes through a priority encode cycle (delay) in which the contents of the flag register *18* are switched over to the second priority flag data held in the prefetch circuit (holding means) after the last hit signal in the flag data in the first priority sub-block held in the flag register is reset; therefore, a time/delay during which no encode output can be performed – between holding and prioritizing stages (col. *22* lines *7-15*).

Consider claim **4**, and as applied to claim **1** above, **Yoneda et al** clearly show and disclose a timing circuit *60* that sends variation of output signals to show a timing at which a flag data in a prefetch circuit *16* is shifted to a flag register *18* in which the flag data held is being encoded with a predetermined priority (col. *25* lines *39-51*; figs. *10-11*).

Consider claim **5**, and as applied to claim **1** above, **Yoneda et al** clearly show

and disclose hit flag data are predetermined into first and second priorities and so on as

non-first priority data are held in a prefetch register and wait (delay) until their priority

comes/the last signal to be output (col. *21* lines *46-67* & col. *22* lines *1-15*; *abstract*).

Therefore, this procedure implies that <u>each</u> output signal is <u>prioritized</u> and <u>delayed</u>.

Consider claim **6**, and as applied to claim **1** above, **Yoneda et al** clearly show

and disclose when priority flag/hit ("1" – <u>highest priority</u>) data moves to another priority

sub-block, the flag data goes through a priority encode cycle (delay) in which the

contents of the flag register *18* are switched over to the second priority flag data held in

the prefetch circuit after the last hit signal in the flag data in the first priority sub-block

held in the flag register is reset; therefore, producing a <u>time/delay</u> during which no

encode <u>output</u> can be performed (col. *22* lines *7-15*).

Consider claim **7**, and as applied to claim **1** above, **Yoneda et al** clearly show

and disclose the timing control circuit, which is a <u>flip-flop circuit</u> as shown in *figure 23* as

D-latch modules *16* and *18*, detects flag data (high/hit signals), <u>held</u> in the flag register

18, applies a switch timing signal or <u>initial value setting signal</u> (as a trigger signal) to the

flag register *18* and feeds the flag data in the prefetch circuit *16* to the flag register (col.

21 lines *46-57*; fig. *23*). A <u>reset signal</u> is also linked to the flag register *18* through an

AND gate *88* and OR gate *114* (col. *28* lines *29-43*; fig. *23*).

Consider claim **8**, and as applied to claim **1** above, **Yoneda et al** clearly show

and disclose priority sub-block encoder – for <u>prioritizing</u> means – <u>gate</u> components AND

gate *88*, OR gate *114,* D-Latches (with <u>gate circuits</u> inside) that <u>hold</u> flag signals, as well

as PMOS and NMOS gates (col. *9* lines *4-5*; fig. *23*).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148

USPQ 459 (1966), that are applied for establishing a background for determining

obviousness under 35 U.S.C. 103(a) are summarized as follows:

1.   Determining the scope and contents of the prior art.
2.   Ascertaining the differences between the prior art and the claims at issue.
3.   Resolving the level of ordinary skill in the pertinent art.
4.   Considering objective evidence present in the application indicating
      obviousness or nonobviousness.

This application currently names joint inventors. In considering patentability of

the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of

the various claims was commonly owned at the time any inventions covered therein

were made absent any evidence to the contrary. Applicant is advised of the obligation

under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was

not commonly owned at the time a later invention was made in order for the examiner to

consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g)

prior art under 35 U.S.C. 103(a).

Claims **3** and **9 – 11** rejected under 35 U.S.C. 103(a) as being unpatentable over

Yoneda et al (U.S Patent 5,726,942) in view of **Okabayashi et al (JP 1993-259900).**

Consider claim **3**, and as applied to claim **2** above, **Yoneda et al** clearly show

and disclose a priority sub-block encoder (priority circuit) that assigns signals as

mismatch ("0" as in invalid/lower priorities) or hit ("1" as in valid/highest priority) in which only

a first priority address matches even though <u>a plurality of matching signal candidates</u>

<u>exist</u> as priority flag/hit data moves to a <u>second/lower</u> priority sub-block (col. *4* lines *5-13*

& col. *11* lines *42-47*; figs. *1-2*). The hit signal data in the second/lower priority sub-block

latch-held in the prefetch circuit is shifted to each corresponding circuit of the data latch

circuit *18* and <u>held</u> therein; and therefore, the transmission of signals are <u>delayed</u> for

<u>lower prioritized</u> signals (col. *12* lines *60-63*).

However, **Yoneda et al** did not specifically disclose a plurality of stages of

inverter circuits connected in series for the delaying means.

In a related field of endeavor, **Okabayashi et al** disclose a circuit comprising an

even number of conduction <u>resistor</u> controlled CMOS inverters (in a plurality) connected

in <u>series</u> (*abstract*; paragraph *0031*; fig. *1* modules *41-44* & block *2*).

Therefore, it would have been obvious to a person of ordinary skill in the art at

the time of the invention was made to incorporate the teachings of a plurality of delay

inverter circuits connected in series as taught by **Okabayashi et al**, in the circuit of

Yoneda et al, for the purpose of creating delay during phase modulation to detect for

potential deviations in output signals.

Consider claim **9**, and as applied to claim **1** above, **Yoneda et al** clearly show

and disclose the delaying and prioritizing means as well as a timing control circuit with a

reset signal and a signal that passes through inverter *84* into a <u>logic AND gate</u> *88* (AND

gate takes the *product* of two inputs); obviously for <u>enabling/disabling</u> the delay operations

(col. *28* lines *29-43*; fig. *23*).

However, **Yoneda et al** did not specifically mention the delay inverter circuits

connected in series comprise PMOS transistors, resistors and NMOS transistors.

In a related field of endeavor, **Okabayashi et al** disclose a circuit employing an

even number of conduction <u>resistor</u> controlled CMOS inverters, which comprise of

PMOS and NMOS transistors, connected in series (*abstract*; paragraph *0031*; fig. *1*

modules *41-44* & block *2*).

Therefore, it would have been obvious to a person of ordinary skill in the art at

the time of the invention was made to incorporate the teachings of a delay inverter

circuits connected in series comprise PMOS transistors, resistors and NMOS transistors

as taught by **Okabayashi et al**, in the circuit of **Yoneda et al**, for the purpose of

creating delay during phase modulation to detect for potential deviations in output

signals.

Consider claim **10**, and as applied to claim **1** above, **Yoneda et al** clearly show

and disclose a timing circuit *60* (acting as a delay circuit) that sends variation of output

signals to show a timing at which a flag data in a prefetch circuit *16* is shifted to a flag

register *18* in which the flag data held is being encoded with a predetermined priority

(col. *25* lines *39-51*; figs. *10-11*).

However, **Yoneda et al** did not specifically disclose the delay circuit having an

even number of stages of delay inverter circuits connected in series, the delay inverter

circuits comprising PMOS transistors, resistors and NMOS transistors.

In a related field of endeavor, **Okabayashi et al** disclose a circuit employing an

even number of conduction resistor controlled CMOS inverters, which comprise of

PMOS and NMOS transistors (well-known in the art), connected in series (*abstract*;

paragraph *0031*; fig. *1* modules *41-44* & block *2*).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention was made to incorporate the teachings of a delay inverter circuits connected in series comprise PMOS transistors, resistors and NMOS transistors as taught by **Okabayashi et al**, in the circuit of **Yoneda et al**, for the purpose of creating delay during phase modulation to detect for potential deviations in output signals.

Consider claim **11**, and as applied to claim **10** above, **Yoneda et al** clearly show and disclose the delaying means of the claimed invention and the timing control circuit that comprises a reset signal and a signal that passes through inverter *84* into a logic AND gate *88* (AND gate takes the *product* of two inputs) and then the product signal passes through a logic OR gate *114* with the initial value setting signal; obviously for enabling/disabling the delay operations (col. *28* lines *29-43*; fig. *23*).

However, **Yoneda et al** did not specifically disclose a plurality of delay circuits each having an even number of stages of delay inverter circuits connected in series, the delay inverter circuits comprising PMOS transistors, resistors and NMOS transistors.

In a related field of endeavor, **Okabayashi et al** disclose a circuit comprising an even number of conduction resistor controlled CMOS inverters (in a plurality), which comprise of PMOS and NMOS transistors, connected in series (*abstract*; paragraph *0031*; fig. *1* modules *41-44* & block *2*).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention was made to incorporate the teachings of a plurality of delay

inverter circuits connected in series comprise PMOS transistors, resistors and NMOS

transistors as taught by **Okabayashi et al**, in the circuit of **Yoneda et al**, for the purpose

of creating delay during phase modulation to detect for potential deviations in output

signals.

Response to Arguments

Applicant's arguments filed 2nd *July 2007* with respect to claims **1-11** have been

considered but are moot in view of the new ground(s) of rejection.

Applicant's arguments filed 2nd *July 2007* with respect to claims **1** has been

considered but they are not persuasive.

Yoneda et al further reads on the amended *limitations as claimed* in claim **1**

(please see examiner's revised claim *1* rejection). The applicants basically argue that

the dependent claims should be patentable because they depend on **Yoneda et al** in

independent claim **1**. This amounts to a general allegation that the claims define a

patentable invention without specifically pointing out how the language of the claims

patentably distinguishes them from the references (please see 37 CFR 1.111(b)).

In view of the above reasons and having addressed the applicant's argument, the

rejection is maintained and made FINAL by the examiner.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in

this Office action. Accordingly, This action is made **FINAL**. See MPEP § 706.07(a).

Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).
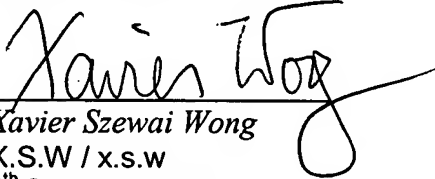
A shortened statutory period for reply to this final action is set to expire THREE

MONTHS from the mailing date of this action. In the event a first reply is filed within

TWO MONTHS of the mailing date of this final action and the advisory action is not

mailed until after the end of the THREE-MONTH shortened statutory period, then the

shortened statutory period will expire on the date the advisory action is mailed, and any

extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later

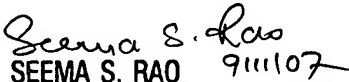than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the

examiner should be directed to Xavier Wong whose telephone number is (571) 270-

1780. The examiner can normally be reached on Monday through Friday 8 am - 5 pm

(EST).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's

supervisor, Seema Rao can be reached on (571) 272-3174. The fax phone number for

the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the

Patent Application Information Retrieval (PAIR) system. Status information for

published applications may be obtained from either Private PAIR or Public PAIR.

Status information for unpublished applications is available through Private PAIR only.

For more information about the PAIR system, see http://pair-direct.uspto.gov. Should

you have questions on access to the Private PAIR system, contact the Electronic

Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a

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system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Xavier Szewai Wong
X.S.W / x.s.w
5th September 2007

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